ATS2835P Datasheet

Actions® ATS2835P™ QFN68

Bluetooth Audio Solution

Low Power Solution for
Portable & Wireless Audio Applications
Local MMC/SD Card Audio Playback

CPU + DSP Dual-core Single-chip
Bluetooth V5.3

Version: V1.4

2022-03-14

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Revision History

Date	Revision	Description
2021-3-20	V1.0	Initial version
2021-8-20	V1.1	Modified
2021-11-10	V1.2	Modified
2021-11-26	V1.3	Modified the GPIO Initial State
2022-03-14	V1.4	Modified the Pin Description

1 Introduction

1.1 Overview

Actions' ATS2835P is a highly integrated single-chip Bluetooth Audio solution. Positioning at Bluetooth portable stereo speakers, headsets and speakerphones and local MMC/SD Card Audio Playback market, ATS2835P satisfies the market requirements with high performance, low cost and low power consumption.

ATS2835P adopts CPU + DSP dual core architecture. Large capacity RAM is embedded to meet different Bluetooth applications, and support Bluetooth background working while playing high quality music with traditional plug-in card and USB flash disk. ATS2835P supports decoding Bluetooth A2DP audio and loading sound effects simultaneously, support Bluetooth handfree calls with dual MIC AEC and noise reduction.

ATS2835P integrates Bluetooth controller support V5.3 and compliant with V5.2/5.0/4.2/2.1 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2835P takes special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS2835P are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market. Above all, ATS2835P provides a true "ALL-IN-ONE" solution, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Key Features

System

- 264MHz RISC-32 CPU processor Core
- 342MHz CEVA DSP core
- Internal 498.5KB RAM for data and program
- Internal 32KB CPU ICache for SPI NorFlash
- Internal 32KB Cache for SPI pSRAM
- Internal 32M bits 4xIO SPI serial Flash for custom defined software
- Up to 16MB extensional pSRAM to support rich and flexible software feature
- Supports 24MHz OSC with on-chip PLL
- Operating voltage: I/O 3.1V, Core 1.2V
- Fully configurable PEQ
- Supports for echo cancellation , noise reduction and wind noise reduction
- Supports for packet loss concealment
- Supports for sound effect, such as MDRC, bass enhancement, virtual surround effects
- Symmetric and asymmetric cryptography
- 128bit efuse is used for symmetric key when using symmetric cryptography
- Asymmetric cryptography signature algorithm is SHA256 With RSA Encryption, the public key is 2048bit

Bluetooth

- Supports Dual-mode Bluetooth V5.3 with LE audio
- Max transmitting output power: 11dBm
- Bluetooth receiving sensitivity: -94dBm@GFSK, -94dBm@π/4 DQPSK, -87dBm@8DPSK modulation
- Compatible with Bluetooth V5.2/V5.0/V4.2/V4.2 LE/V4.0/V3.0/V2.1 + EDR systems
- Compatible with AVRCP Profile V1.6.2
- Compatible with A2DP Profile V1.3.2
- Compatible with HFP Profile V1.8
- Support for SBC & AAC Bluetooth audio transmission format
- Support for mSBC broadband speech coding
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class1 PA
- Supports connecting external PA
- Supports Power / Enhanced Power Control

Package

- QFN-68 (8mm*8mm, Pitch 0.4mm)

Audio

- Built-in stereo 24 bit input sigma-delta DAC
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1/48/96kHz
- Built-in stereo 20mW PA for headphone. PA output supports traditional mode and direct drive mode (for earphone)
- Supports differential audio output
- Built-in stereo 24 bit input sigma-delta ADC
- ADC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48/96kHz
- Supports 3 stereo single-ended analog input or 1 stereo fully differential analog input plus 1 stereo single-ended analog input
- Supports Digital microphones
- Supports single-ended Analog microphones and fully differential microphone
- Audio Interfaces: I2S TX and I2S RX*2, sampling rate up to 192KHz
- Audio Interfaces: SPDIF TX and RX, sampling rate up to 96KHz

Power Management

- Supports Li-Ion battery and 5V power supply
- Integrated DC-DC buck converters
- Linear regulators output VCC, SVCC, RTCVDD
- Standby Leakage Current (Include RTC module):<50uA(Whole System)
- Low Power Consumption:
  Typical Sniff Current: 450uA@Vbat=3.8V
  A2DP: 13.5mA@Vbat=3.8V, SBC;
  HFP: 16.5mA@Vbat=3.8V, mSBC;

Physical Interfaces

- Supports SD/MMC/eMMC card interface
- Supports SDIO interface

- USB 2.0 device and host controllers
- Serial Interface: SPI*2, UART*2, TWI
- Supports Remote Control with internal IRC
- Supports LCM with 8bit CPU Interface, 4COM/5COM/6COM Segment LCD, 7pin LED
- 9 PWM drivers independent of MCU

Applications

- Portable stereo speakers and speakerphones
- Bluetooth car audio unit
- Stereo headsets and headphones
- Other Bluetooth audio applications

1.3 Application Diagram

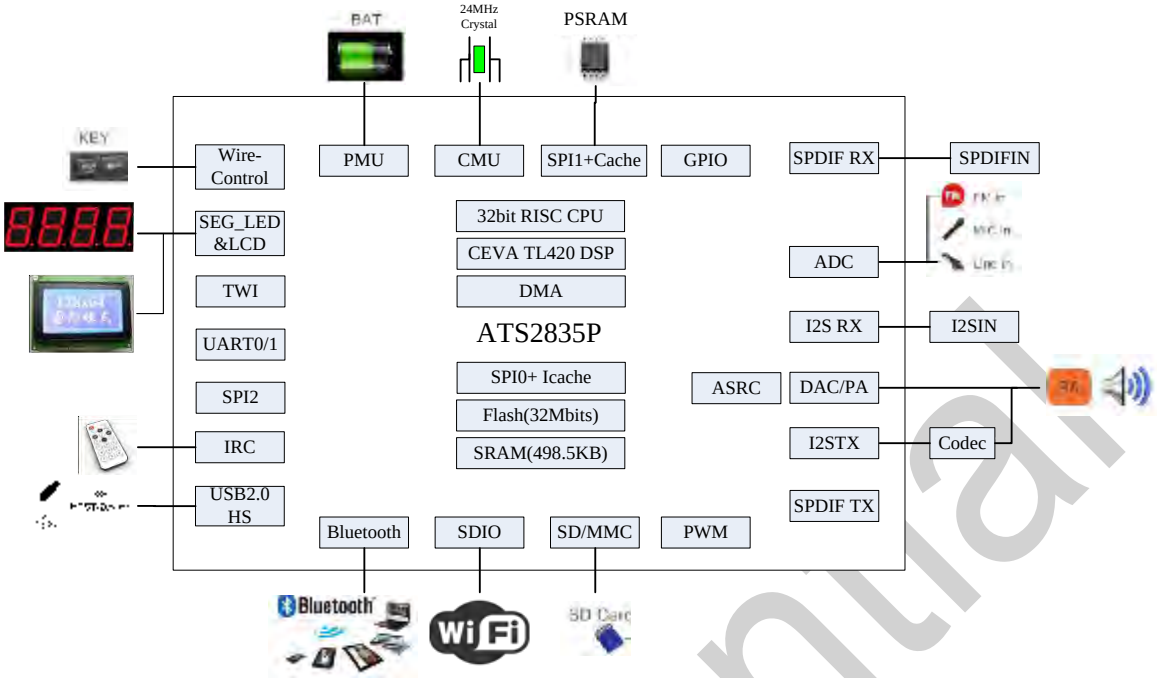
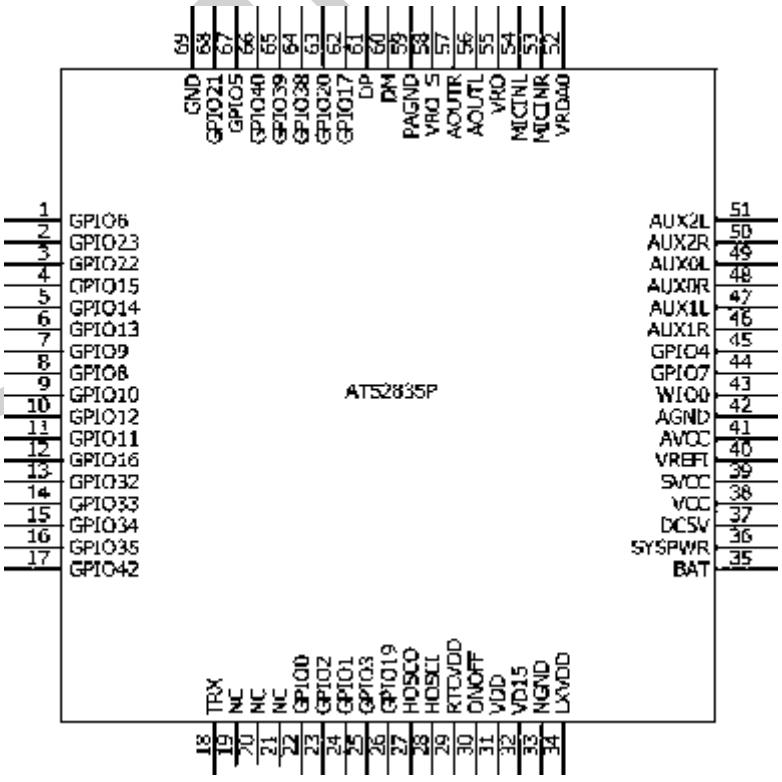


Figure 1-1 ATS2835P Application Diagram

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment



1.4.2 Pin Description

Pin No.	Pin Name	Function Multiplex	IO Type	PAD Drive Level	GPIO Initial State	Description
1	GPIO6	LED_COM6 BT_ACCESS LCD_SEG0 PWM4 I2STX0_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SD1_DAT0	DIO	2/4/6/8/10/12/14/16mA	Z	Bit6 of General purpose I/O port
2	GPIO23	LCD_D11 LCD_SEG13 SPDIF_TX PWM2 UART0_TX LRADC3 I2STX0_BCLK I2SRX0_BCLK I2SRX1_BCLK Timer3_cap SD1_CMD SD0_DAT3 SD0_DAT0	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade(V), Firmware boot(Z)	Bit23 of General purpose I/O port
3	GPIO22	LCD_D10 LCD_SEG12 IR_RX PWM1 UART0_TX LRADC2 I2STX0_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SD1_DAT2 UART1_RX SD0_DAT2	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade(V), Firmware boot(Z)	Bit22 of General purpose I/O port
4	GPIO15	LED_SEG7 LCD_D7 LCD_SEG9 SPI1_IO3 PWM4 UART1_RX I2STX0_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer3_cap SD1_DAT0 SPI0_IO3	DIO	2/4/6/8/10/12/14/16mA	Z	Bit15 of General purpose I/O port
5	GPIO14	LED_SEG6 LCD_D6	DIO	2/4/6/8/10/12/14/16mA	Z	Bit14 of General purpose I/O port

		LCD_SEG8 SPI1_IO2 LRADC11 SPI0_IO2 Timer2_cap				
6	GPIO13	LED_SEG5 LCD_D5 LCD_SEG7 SPI1_IO3 PWM8 UART1_RTS LRADC10 SPI0_IO3 Timer3_cap SD1_DAT3	DIO	2/4/6/8/10/12/14/16mA	Z	Bit13 of General purpose I/O port
7	GPIO9	LED_SEG1 LCD_D1 LCD_SEG3 SPI1_CLK PWM4 LRADC6 SPI0_SCLK SPI2_CLK Timer3_cap SD1_CMD	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit9 of General purpose I/O port
8	GPIO8	LED_SEG0 LCD_D0 LCD_SEG2 SPI1_SS PWM3 LRADC5 SPI0_SS SPI2_SS Timer2_cap SD1_CLK	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit8 of General purpose I/O port
9	GPIO10	LED_SEG2 LCD_D2 LCD_SEG4 SPI1_MISO PWM5 UART0_CTS LRADC7 SPI0_MISO SPI2_MISO Timer2_cap SD1_DAT0	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit10 of General purpose I/O port
10	GPIO12	LED_SEG4 LCD_D4 LCD_SEG6 SPI1_IO2 PWM7 LRADC9 SPI0_IO2 Timer2_cap	DIO	2/4/6/8/10/12/14/16mA	Z	Bit12 of General purpose I/O port

		SD1_DAT2				
11	GPIO11	LED_SEG3 LCD_D3 LCD_SEG5 SPI1_MOSI PWM6 UART0_RTS LRADC8 SPI0_MOSI SPI2_MOSI Timer3_cap SD1_DAT1 BT_ACCESS	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit11 of General purpose I/O port
12	GPIO16	SPI2_SS LCD_SEG14 SPI1_SS PWM4 UART0_RX Timer2_cap SD0_CMD	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit16 of General purpose I/O port
13	GPIO32	LCD_SEG22 I2STX0_MCLK I2SRX0_MCLK I2SRX1_MCLK VMIC	DIO	2/4/6/8/10/12/14/16mA	PU	Bit32 of General purpose I/O port
14	GPIO33	LCD_SEG23 I2STX0_BCLK I2SRX0_BCLK I2SRX1_BCLK	DIO	2/4/6/8/10/12/14/16mA	PU	Bit33 of General purpose I/O port
15	GPIO34	LCD_SEG24 I2STX0_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK BT_REQ	DIO	2/4/6/8/10/12/14/16mA	PU	Bit34 of General purpose I/O port
16	GPIO35	SPDIF_TX LCD_SEG25 I2STX0_DOUT I2SRX0_DIN I2SRX1_DIN	DIO	2/4/6/8/10/12/14/16mA	Z	Bit35 of General purpose I/O port
17	GPIO42	TWI_SCL PWM3 PWM5 I2STX0_BCLK I2SRX0_BCLK I2SRX1_BCLK SD0_CLK0 IR_RX UART1_TX SD1_DAT1	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit42 of General purpose I/O port
18	TRX		RF			Bluetooth antenna IO
19	NC					NC

20	NC					NC
21	NC					NC
22	GPIO0	LED_COM0 LCD_WRB LCD_COM0 TWI_SCL PWM1 UART0_RTS I2STX0_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer2_cap SPI2_SS	DIO	2/4/6/8/10/ 12/14/16mA	Z	Bit0 of General purpose I/O port
23	GPIO2	LED_COM2 LCD_RDB LCD_COM2 SPI1_MOSI PWM2 UART0_RX LRADC4 I2STX0_LRCLK I2SRX0_LRCLK I2SRX1_LRCLK Timer2_cap SPI2_MOSI	DIO	2/4/6/8/10/ 12/14/16mA	V	Bit2 of General purpose I/O port
24	GPIO1	LED_COM1 LCD_RS LCD_COM1 TWI_SDA PWM3 UART0_CTS I2STX0_BCLK I2SRX0_BCLK I2SRX1_BCLK Timer3_cap SPI2_MISO	DIO	2/4/6/8/10/ 12/14/16mA	Z	Bit1 of General purpose I/O port
25	GPIO3	LED_COM3 LCD_CEB LCD_COM3 SPI1_CLK UART0_TX I2STX0_DOUT I2SRX0_DIN I2SRX1_DIN Timer3_cap SPI2_CLK	DIO	2/4/6/8/10/ 12/14/16mA	V	Bit3 of General purpose I/O port
26	GPIO19	LCD_SEG17 TWI_SDA Timer3_cap	DIO	2/4/6/8/10/ 12/14/16mA	Z	Bit19 of General purpose I/O port
27	HOSCO		AO			24MHz clock output
28	HOSCI		AI			24MHz clock input
29	RTCVDD		PWR			RTC power
30	ONOFF		AI			ON/OFF reset signal
31	VDD		PWR			Core Logic PWR

32	VD15		PWR			1.5V DCDC feedback
33	NGND		GND			GND
34	LXVDD		PWR			DCDC Output
35	BAT		PWR			Battery Voltage input
36	SYSPWR		PWR			System PWR
37	DC5V		PWR			5.0V Voltage
38	VCC		PWR			Digital IO PWR
39	SVCC		PWR			PWR for standby
40	VREFI		PWR			Reference voltage input
41	AVCC		PWR			Analog IO PWR
42	AGND		GND			Analog GND
43	WIO0	EXT_32K_IN HOSC LRADC1	DIO	2/4/6/8/10/ 12/14/16mA	Z	Wake up I/O port
44	GPIO7	LED_COM7 PTA_GRANT LCD_SEG1 SPDIF_RX PWM0 UART1_TX FMCLKOUT I2STX0_DOUT I2SRX0_DIN I2SRX1_DIN Timer3_cap SD1_DAT3	DIO	2/4/6/8/10/ 12/14/16mA	Z	Bit7 of General purpose I/O port
45	GPIO4	LED_COM4 LCD_CEB LCD_COM4 PWM1 Timer2_cap IR_RX VMIC	DIO	2/4/6/8/10/ 12/14/16mA	Z	Bit4 of General purpose I/O port
46	AUX1R/ AUXR	GPIO49	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM right channel input1, right channel differential input
47	AUX1L/ AUXR	GPIO48	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM left channel input1, right channel differential input
48	AUX0R/ AUXL	GPIO47	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM right channel input0, left channel differential input
49	AUX0L/ AUXL	GPIO46	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM left channel input0, left channel differential input
50	AUX2R	GPIO55	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM right channel input2
51	AUX2L	GPIO54	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Linein/FM left channel input2
52	VRDA		PWR			AUDIO power
53	MICINR/ MICINN	GPIO45 DMIC_DAT	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Microphone right channel input, Differential MICIN Negative Input
54	MICINL/ MICINP	GPIO44 DMIC_CLK	AI/DIO	2/4/6/8/10/ 12/14/16mA	Z	Microphone left channel input, Differential MICIN Positive Input
55	AOUTLN/ VRO	GPIO51 I2STX_LRCLK	AO/DIO	2/4/6/8/10/ 12/14/16mA	Z	Left channel differential output and direct drive circuit reference

		I2SRX0_LRCLK I2SRX1_LRCLK PWM3				voltage
56	AOUTL/ AOUTLP	GPIO50	AO/DIO	2/4/6/8/10/ 12/14/16mA	Z	Left channel output and left channel differential output
57	AOUTR/ AOUTRP	GPIO52	AO/DIO	2/4/6/8/10/ 12/14/16mA	Z	Right channel output and right channel differential output
58	AOUTRN/ VRO_S	GPIO53 I2STX_DOUT I2SRX0_DIN I2SRX1_DIN PWM5	AO/DIO	2/4/6/8/10/ 12/14/16mA	Z	Right channel differential output and direct drive circuit reference voltage
59	PAGND		GND			GND for PA
60	HSDM		AIO		V	USB Data minus
61	HSDP		AIO		V	USB Data plus
62	GPIO17	SPI2_CLK LCD_SEG15 SPI1_CLK UART0_TX Timer3_cap SD0_CLK0	DIO	2/4/6/8/10/ 12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit17 of General purpose I/O port
63	GPIO20	SPI2_MISO LCD_D8 LCD_SEG10 SPI1_MISO PWM2 UART1_CTS Timer2_cap SD0_DAT0 VMIC	DIO	2/4/6/8/10/ 12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit20 of General purpose I/O port
64	GPIO38	SPDIF_RX BT_REQ LCD_SEG28 PWM0 I2STX0_DOUT I2SRX0_DIN I2SRX1_DIN	DIO	2/4/6/8/10/ 12/14/16mA	PU	Bit38 of General purpose I/O port
65	GPIO39	BT_ACCESS LCD_SEG29 PWM1 I2STX0_BCLK I2SRX0_BCLK I2SRX1_BCLK	DIO	2/4/6/8/10/ 12/14/16mA	PU	Bit39 of General purpose I/O port
66	GPIO40	PTA_GRANT LCD_SEG30 PWM2 I2STX0_MCLK I2SRX0_MCLK I2SRX1_MCLK	DIO	2/4/6/8/10/ 12/14/16mA	PU	Bit40 of General purpose I/O port

67	GPIO5	LED_COM5 BT_REQ LCD_COM5 PWM3 Timer3_cap	DIO	2/4/6/8/10/12/14/16mA	Z	Bit5 of General purpose I/O port
68	GPIO21	SPI2_MOSI LCD_D9 LCD_SEG11 SPI1_MOSI PWM0 UART0_RX TEMPADC I2STX0_MCLK I2SRX0_MCLK I2SRX1_MCLK Timer3_cap SD1_CLK UART1_TX SD0_DAT1	DIO	2/4/6/8/10/12/14/16mA	Firmware upgrade (V), Firmware boot(Z)	Bit21 of General purpose I/O port
69	EPAD		GND			Exposed pad as ground

Note:

(1) Boot from SPI Nor Flash;

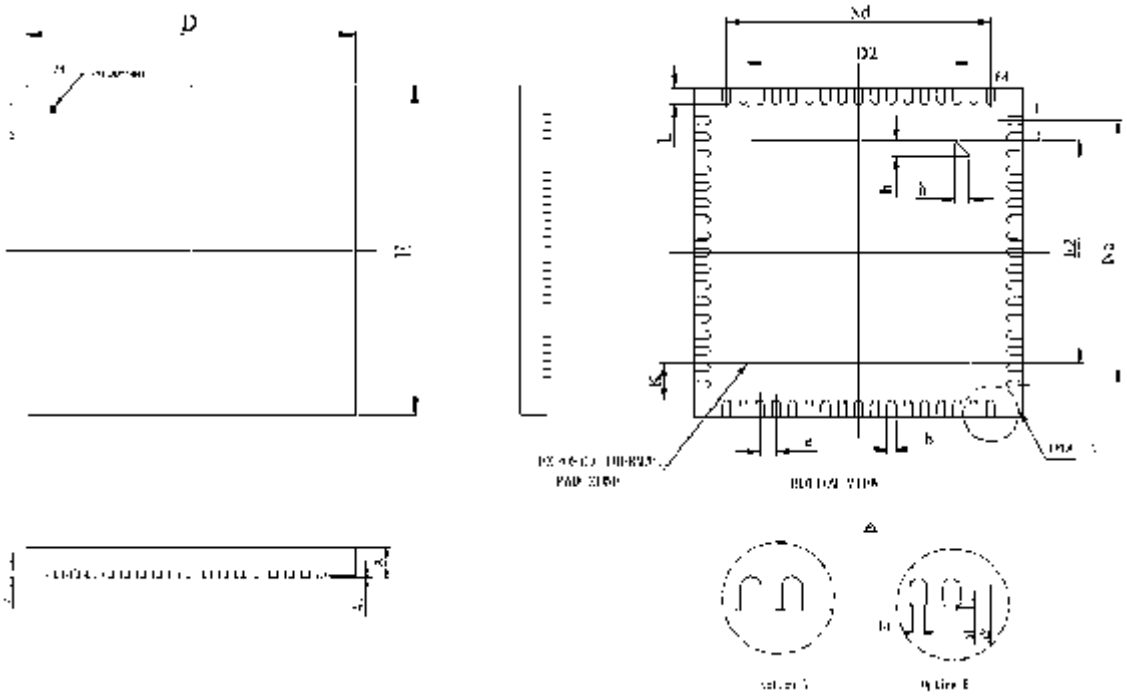
(2) PU: Pull up through 10K resistor;

(3) Z: High resistance;

(4) V: Variable state;

(5) L: Low level.

1.4.3 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90
	0.85	0.90	0.95
A1		0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.27
D	7.90	8.00	8.10
e	0.40BSC		
Nd	3.60BSC		
E	7.90	8.00	8.10
Ne	3.60BSC		
L	0.35	0.40	0.45
L1	0.20	—	—
h	0.30	0.35	0.40
h1	0.04REF		
h2	0.10REF		
J2	3.26	3.49	3.59
J2	3.26	3.49	3.59

2 Bluetooth

2.1 Features

- Supports Dual-mode Bluetooth V5.3 with LE audio
- Compatible with Bluetooth V5.2/V5.0/V4.2/V4.2 LE/V3.0/V2.1 +EDR systems
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Class1 transmit output power supported
- Supports GFSK, π/4 DQPSK and 8DPSK modulation
- Supports Power / Enhanced Power Control
- LE Data Packet Length Extension
- LE 2M PHY
- Channel Selection Algorithm #2

2.2 Bluetooth Performance

- Max transmitting output power: 11dBm
- Bluetooth receiving sensitivity: -94dBm@GFSK, -94dBm@π/4 DQPSK, -87dBm@8DPSK modulation

3 Processor Core

- 264MHz(typical) RISC-32 CPU processor Core
- 32-bit Address and Data Paths

- RISC reduced instruction structure
- 32 bit data, 16/32 bit mixed coding command

4 DSP Core

- 342MHz CEVA TL420 DSP core
- High code compactness
- All instructions can be conditional
  - Conditional execution
  - Reduces cycle count and code size on control and overhead code
- Computational units:
  - One 32-bit x 32-bit Multiply-and-Accumulate (MAC) using 72-bit product
  - One 32-bit x 16-bit MAC using 72-bit product
  - One 32-bit x 32-bit MAC unit with automatic scaling
  - One 32-bit x 16-bit MAC unit with automatic scaling
  - One 36-bit arithmetic unit
  - One 36-bit logical unit
  - One 36-bit bit-manipulation unit, including a full barrel shifter and an exponent unit
  - Four 36-bit accumulators
  - Fully programmable product post-shifter for product scaling
- 32-bit Scalar (SC) unit for integer operations
- Unaligned memory access for load and store operations

5 Memory Controller

- Internal 32KB CPU ICache for SPI NorFlash
- Internal 498.5KB SRAM for data and program
- Internal 32KB Cache for SPI pSRAM, which can be switched to 32K SRAM when Cache is useless.
- Internal 32M bits 4xIO SPI serial Flash for custom defined software
- Up to 16M bytes extensional pSRAM to support rich and flexible soft feature
- It is accessible for all the RAM blocks through DMA
- It is accessible for all the RAM blocks through DSP's data bus and program bus
- It is accessible for all the RAM and ROM block through CPU I/D bus
- The hardware code replace mechanism can fix up to 4 instructions at the same time
- The page miss control mechanism can support 16 different pages at the same time

6 DMA Controller

6.1 Features

- DMA transmission is independent with the CPU and DSP
- Support for memory to memory, memory to peripheral, peripheral to memory, CARD to USB, and USB to CARD transmission.
- 8-channel ordinary DMA, that supports for transmission in burst 8 mode or single mode. Only one of the eight DMA channels can transfer data at the same time.
- DMA0-7 transmission can be triggered on the occurrence of selected events
- Each channel can send two interrupts to the CPU on completion of certain operational events
- Transmission width includes 8-bit, 16-bit, and 32-bit, which is determined by DMA transmission type.

6.2 Memory and Peripheral Access Description

6.2.1 Access memory

（1） Memory is accessed by DMA according to physical address.

（2） The following situations will lead to transfer error:
- Access rom
- Ram has been occupied by other modules
- The clock of ram is disabled

（3） DMA can access pSRAM by CACHE mode or UNCACHE mode. The DMASADDR and DMADADDR must both be pSRAM or Internal RAM when using the AUDIO separated type to transfer.

（4） Memory-to-memory transmission:
- The data in memory should be aligned by word (32-bit) when transferred.
- The transfer width is 64-bit when both the source and destination address are aligned by double-word (64-bit), otherwise the transfer width is 32-bit.

（5） Memory-to-peripheral and peripheral-to-memory transmission:
- The data in memory should be aligned by word (32-bit) when the transfer width is 32-bit or 24-bit.
- The data in memory should be aligned by half-word (16-bit) when the transfer width is 16-bit.
- The data in memory should be aligned by byte (8-bit) when the transfer width is 8-bit.

（6） SRCTYPE/ DSTTYPE/SADDR/DADDR should be set when DMA access the peripherals.

（7） CPU cannot access the peripherals FIFO when the peripherals FIFO is accessed by DMA.

6.2.2 Access Peripheral FIFO

The peripherals that can be accessed by DMA are shown as following:

FIFO Type	FIFO Width	FIFO Depth
SPI0 TX FIFO	8	16
SPI0 RX FIFO	8	16
UART0/1 TX FIFO	8	16
UART0/1 RX FIFO	8	16
USB FIFO	8/32	8
SD/MMC FIFO	32	128
SDIO	32	128
LCD FIFO	16	8
I2S TX/DAC/SPDIF TX FIFO0(DACFIFO0)	16/24(32)	32
I2S TX/DAC/SPDIF TX FIFO1(DACFIFO1)	16/24(32)	32
I2S TX/SPDIF TX FIFO(I2STXFIFO)	16/24(32)	32
I2S RX0/ADC FIFO(ADCFIFO)	16/24(32)	32
I2S RX1/SPDIF RX FIFO(I2SRX1FIFO)	16/24(32)	32
SPI1 TX FIFO	8/32	16
SPI1 RX FIFO	8/32	16
SPI2 TX FIFO	8/32	16
SPI2 RX FIFO	8/32	16

6.2.3 Access Peripheral Mode

Peripheral	Single	Burst8
SPI0	Y	Y
UART0/1	Y	Y
USB	Y	Y

SD/MMC	N	Y
SDIO	N	Y
LCD	N	Y
I2STX/DAC/SPDIFTX	N	Y
I2SRX0/ADC	N	Y
I2SRX1/SPDIFRX	N	Y
SPI1	Y	Y
SPI2	Y	Y

6.2.4 DMA channel priority

Each memory block can be accessed by only one of the three masters at the same time, which are DSP, CPU, and DMA. The 8 channels of DMA share the same bus, so only one of these channels can use the bus to transfer data at the same moment.

While accessing one memory block, DMA submits an access request to the memory controller's arbiter. Meanwhile, DSP or CPU might send another request to access the same memory block. The arbiter grants the bus of this memory block according to the priority scheme. The priority scheme is known as round-robin algorithm. When DMA does not get the bus of this memory block, the memory controller will hold DMA. See memory controller specification for details.

Once DMA obtains the highest priority among the three masters, one of the 6 channels occupies the DMA bus according to the internal priority. The priority of DMA channel is DMA0 > DMA1 > DMA2 > DMA3 > DMA4 > DMA5 > DMA6 > DMA7.

6.2.5 DMA Access Channel

DMA supports memory-to-memory, memory-to-peripheral, and peripheral-to-memory transmission. Specific access paths are shown as follows:

DST / SRC	RAM	SPI0/1/2 TX FIFO	UART0 UART1 TX FIFO	USB FIFO	SDIO FIFO	SD/ MMC FIFO	LCD FIFO	I2S TX (SPDIFTX/ DAC) FIFO0/1	I2S TX/ SPDIFTX FIFO	pSRAM
RAM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
SPI0/1/2 RX FIFO	Y	-	-	-		-	-	-		Y
UART0/1 RX FIFO	Y	-	-	-		-	-	-		Y
USB FIFO	Y	-	-	-		Y	-	-		Y
SDIO	Y									Y
SD/MMC FIFO	Y	-	-	Y		-	-	-		Y
LCD FIFO	Y	-	-	-		-	-	-		Y
I2S RX0 (ADC)FIFO	Y	-	-	-		-	-	-		Y
I2S RX1 SPDIF RX FIFO	Y									Y
pSRAM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

6.3 DMA Register List

Table 6-1 DMA controller base address

Name	Physical Base Address	KSEG1 Base Address
DMA Controller	0xC0040000	0xC0040000

Table 6-2 DMA controller register list

Offset	Register Name	Description
0x00000000	DMAIP	DMA interrupt pending register
0x00000004	DMAIE	DMA interrupt enable register
0x00000008	DMATIMEOUTPD	DMA time out Pending register
0x00000100	DMA0CTL	DMA0 control register
0x00000104	DMA0START	DMA0 start register
0x00000108	DMA0SADDR0	DMA0 source address register 0
0x0000010c	DMA0SADDR1	DMA0 source address register 1
0x00000110	DMA0DADDR0	DMA0 destination address register 0
0x00000114	DMA0DADDR1	DMA0 destination address register 1
0x00000118	DMA0BC	DMA0 byte counter register
0x0000011C	DMA0RC	DMA0 Remain counter Register
0x00000200	DMA1CTL	DMA1 control register
0x00000204	DMA1START	DMA1 start register
0x00000208	DMA1SADDR0	DMA1 source address register 0
0x0000020C	DMA1SADDR1	DMA1 source address register 1
0x00000210	DMA1DADDR0	DMA1 destination address register 0
0x00000214	DMA1DADDR1	DMA1 destination address register 1
0x00000218	DMA1BC	DMA1 byte counter register
0x0000021C	DMA1RC	DMA1 Remain counter Register
0x00000300	DMA2CTL	DMA2 control register
0x00000304	DMA2START	DMA2 start register
0x00000308	DMA2SADDR0	DMA2 source address register 0
0x0000030C	DMA2SADDR1	DMA2 source address register 1
0x00000310	DMA2DADDR0	DMA2 destination address register 0
0x00000314	DMA2DADDR1	DMA2 destination address register 1
0x00000318	DMA2BC	DMA2 byte counter register
0x0000031C	DMA2RC	DMA2 Remain counter Register
0x00000400	DMA3CTL	DMA3 control register
0x00000404	DMA3START	DMA3 start register
0x00000408	DMA3SADDR0	DMA3 source address register 0
0x0000040C	DMA3SADDR1	DMA3 source address register 1
0x00000410	DMA3DADDR0	DMA3 destination address register 0
0x00000414	DMA3DADDR1	DMA3 destination address register 1
0x00000418	DMA3BC	DMA3 byte counter register
0x0000041C	DMA3RC	DMA3 Remain counter Register
0x00000500	DMA4CTL	DMA4 control register
0x00000504	DMA4START	DMA4 start register
0x00000508	DMA4SADDR0	DMA4 source address register 0
0x0000050C	DMA4SADDR1	DMA4 source address register 1
0x00000510	DMA4DADDR0	DMA4 destination address register 0
0x00000514	DMA4DADDR1	DMA4 destination address register 1
0x00000518	DMA4BC	DMA4 byte counter register
0x0000051C	DMA4RC	DMA4 Remain counter Register
0x00000600	DMA5CTL	DMA5 control register
0x00000604	DMA5START	DMA5 start register
0x00000608	DMA5SADDR0	DMA5 source address register 0
0x0000060C	DMA5SADDR1	DMA5 source address register 1
0x00000610	DMA5DADDR0	DMA5 destination address register 0
0x00000614	DMA5DADDR1	DMA5 destination address register 1

0x00000618	DMA5BC	DMA5 byte counter register
0x0000061C	DMA5RC	DMA5 Remain counter Register
0x00000700	DMA6CTL	DMA6 control register
0x00000704	DMA6START	DMA6 start register
0x00000708	DMA6SADDR0	DMA6 source address register 0
0x0000070C	DMA6SADDR1	DMA6 source address register 1
0x00000710	DMA6DADDR0	DMA6 destination address register 0
0x00000714	DMA6DADDR1	DMA6 destination address register 1
0x00000718	DMA6BC	DMA6 byte counter register
0x0000071C	DMA6RC	DMA6 Remain counter Register
0x00000800	DMA7CTL	DMA7 control register
0x00000804	DMA7START	DMA7 start register
0x00000808	DMA7SADDR0	DMA7 source address register 0
0x0000080C	DMA7SADDR1	DMA7 source address register 1
0x00000810	DMA7DADDR0	DMA7 destination address register 0
0x00000814	DMA7DADDR1	DMA7 destination address register 1
0x00000818	DMA7BC	DMA7 byte counter register
0x0000081C	DMA7RC	DMA7 Remain counter Register

6.4 DMA Register Description

6.4.1 DMAIP

DMA Interrupt Pending Register, offset = 0x00000000

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DMA7HFIP	DMA7 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
14	DMA6HFIP	DMA6 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
13	DMA5HFIP	DMA5 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
12	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
7	DMA7TCIP	DMA7 Transmission Complete IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
6	DMA6TCIP	DMA6 Transmission Complete IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
5	DMA5TCIP	DMA5 Transmission Complete IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written ‘1’ to clear.	R/W	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending	R/W	0x0

		This bit can be written '1' to clear.		
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	R/W	0x0

6.4.2 DMAIE

DMA Interrupt Enable Register, offset = 0x00000004

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DMA7HFIE	DMA7 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
14	DMA6HFIE	DMA6 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
13	DMA5HFIE	DMA5 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
12	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable 0: Disable Half Transmission Complete interrupt 1: Enable Half Transmission Complete interrupt	R/W	0x0
7	DMA7TCIE	DMA7 Transmission Complete IRQ Enable 0: disable DMA7 Transmission Complete interrupt 1: enable DMA7 Transmission Complete interrupt	R/W	0x0
6	DMA6TCIE	DMA6 Transmission Complete IRQ Enable 0: disable DMA6 Transmission Complete interrupt 1: enable DMA6 Transmission Complete interrupt	R/W	0x0
5	DMA5TCIE	DMA5 Transmission Complete IRQ Enable 0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt	R/W	0x0
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt	R/W	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	R/W	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable	R/W	0x0

		0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt		
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	R/W	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	R/W	0x0

6.4.3 DMATIMEOUTPD

DMA Timeout Pending Register, offset = 0x00000008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R/W	0x0
7	DMA7TOPD	DMA7 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
6	DMA6TOPD	DMA6 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
5	DMA5TOPD	DMA5 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
4	DMA4TOPD	DMA4 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
3	DMA3TOPD	DMA3 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
2	DMA2TOPD	DMA2 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
1	DMA1TOPD	DMA1 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0
0	DMA0TOPD	DMA0 Tansmission Time out Pending This bit can be written '1' to clear.	R/W	0x0

6.4.4 DMA0CTL

DMA0 control Register, offset = 0x00000100

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0

12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0 (DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1 (DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.5 DMA0START

DMA0 Start Register 0, offset = 0x00000104

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.6 DMA0SADDR0

DMA0 Source Address Register 0, offset = 0x00000108

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.7 DMA0SADDR1

DMA0 Source Address Register 1, offset = 0x0000010C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.8 DMA0DADDR0

DMA0 Destination Address Register 0, offset = 0x00000110

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.9 DMA0DADDR1

DMA0 Destination Address Register 1, offset = 0x00000114

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.10 DMA0BC

DMA0 Byte Counter Register, offset = 0x00000118

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA0 transmission	R/W	0x0

6.4.11 DMA0RC

DMA0 Remain Byte Counter Register, offset = 0x0000011C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA0 transmission	R/W	0x0

6.4.12 DMA1CTL

DMA1 control Register, offset = 0x00000200

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0

16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0 (DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1 (DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO (ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.13 DMA1START

DMA1 Start Register 0, offset = 0x00000204

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.14 DMA1SADDR0

DMA1 Source Address Register 0, offset = 0x00000208

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.15 DMA1SADDR1

DMA1 Source Address Register 1, offset = 0x0000020C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.16 DMA1DADDR0

DMA1 Destination Address Register 0, offset = 0x00000210

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.17 DMA1DADDR1

DMA1 Destination Address Register 1, offset = 0x00000214

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA1 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.18 DMA1BC

DMA1 Byte Counter Register, offset = 0x00000218

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA1 transmission	R/W	0x0

6.4.19 DMA1RC

DMA1 Remain Byte Counter Register, offset = 0x0000021C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA1 transmission	R/W	0x0

6.4.20 DMA2CTL

DMA2 control Register, offset = 0x00000300

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select	R/W	0x0

		4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved		

6.4.21 DMA2START

DMA2 Start Register 0, offset = 0x00000304

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.22 DMA2SADDR0

DMA2 Source Address Register 0, offset = 0x00000308

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.23 DMA2SADDR1

DMA2 Source Address Register 1, offset = 0x0000030C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.24 DMA2DADDR0

DMA2 Destination Address Register 0, offset = 0x00000310

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.25 DMA2DADDR1

DMA2 Destination Address Register 1, offset = 0x00000314

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA2 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.26 DMA2BC

DMA2 Byte Counter Register, offset = 0x00000318

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA2 transmission	R/W	0x0

6.4.27 DMA2RC

DMA2 Remain Byte Counter Register, offset = 0x0000031C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA2 transmission	R/W	0x0

6.4.28 DMA3CTL

DMA3 control Register, offset = 0x00000400

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO	R/W	0x0

		4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved		
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.29 DMA3START

DMA3 Start Register 0, offset = 0x00000404

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.30 DMA3SADDR0

DMA3 Source Address Register 0, offset = 0x00000408

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.31 DMA3SADDR1

DMA3 Source Address Register 1, offset = 0x0000040C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.32 DMA3DADDR0

DMA3 Destination Address Register 0, offset = 0x00000410

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.33 DMA3DADDR1

DMA3 Destination Address Register 1, offset = 0x00000414

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA3 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.34 DMA3BC

DMA3 Byte Counter Register, offset = 0x00000418

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA3 transmission	R/W	0x0

6.4.35 DMA3RC

DMA3 Remain Byte Counter Register, offset = 0x0000041C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA3 transmission	R/W	0x0

6.4.36 DMA4CTL

DMA4 control Register, offset = 0x00000500

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0

15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.37 DMA4START

DMA4 Start Register 0, offset = 0x00000504

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load	R/W	0x0

		source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.		

6.4.38 DMA4SADDR0

DMA4 Source Address Register 0, offset = 0x00000508

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.39 DMA4SADDR1

DMA4 Source Address Register 1, offset = 0x0000050C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.40 DMA4DADDR0

DMA4 Destination Address Register 0, offset = 0x00000510

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.41 DMA4DADDR1

DMA4 Destination Address Register 1, offset = 0x00000514

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA4 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.42 DMA4BC

DMA4 Byte Counter Register, offset = 0x00000518

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA4 transmission	R/W	0x0

6.4.43 DMA4RC

DMA4 Remain Byte Counter Register, offset = 0x0000051C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCO	The remain counter length of DMA4 transmission	R/W	0x0

	UNTER			

6.4.44 DMA5CTL

DMA5 control Register, offset = 0x00000600

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO	R/W	0x0

		4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved		

6.4.45 DMA5START

DMA5 Start Register 0, offset = 0x00000604

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.46 DMA5SADDR0

DMA5 Source Address Register 0, offset = 0x00000608

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.47 DMA5SADDR1

DMA5SADDR1 (DMA5 Source Address Register 1, offset = 0x0000060c)

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.48 DMA5DADDR0

DMA5 Destination Address Register 0, offset = 0x00000610

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.49 DMA5DADDR1

DMA5 Destination Address Register 1, offset = 0x00000614

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA5 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.50 DMA5BC

DMA5 Byte Counter Register, offset = 0x00000618

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA5 transmission	R/W	0x0

6.4.51 DMA5RC

DMA5 Remain Byte Counter Register, offset = 0x0000061C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA5 transmission	R/W	0x0

6.4.52 DMA6CTL

DMA6 control Register, offset = 0x00000700

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit 3: 8bit	R/W	0x0
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX)	R/W	0x0

		4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved		
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.53 DMA6START

DMA6 Start Register 0, offset = 0x00000704

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.54 DMA6SADDR0

DMA6 Source Address Register 0, offset = 0x00000708

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.55 DMA6SADDR1

DMA6 Source Address Register 1, offset = 0x0000070C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.56 DMA6DADDR0

DMA6 Destination Address Register 0, offset = 0x00000710

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.57 DMA6DADDR1

DMA6 Destination Address Register 1, offset = 0x00000714

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA6 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.58 DMA6BC

DMA6 Byte Counter Register, offset = 0x00000718

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA6 transmission	R/W	0x0

6.4.59 DMA6RC

DMA6 Remain Byte Counter Register, offset = 0x0000071C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA6 transmission	R/W	0x0

6.4.60 DMA7CTL

DMA7 control Register, offset = 0x00000800

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17	TRM	DMA Transfer Mode 0:Burst8 1:Single	R/W	0x0
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, and DMA-I2S transmission 0: interleaved stored in the memory 1: separated stored in the memory	R/W	0x0
15	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	R/W	0x0
14:13	TWS	Transmit data width select 0: 64bit 1: 32bit 2: 16bit	R/W	0x0

		3: 8bit		
12	DAM	Destination address mode 0: increment 1: constant	R/W	0x0
11:8	DSTSL	Destination select 4'b0000: memory 4'b0010: SPI2 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: UART1 TX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 TX FIFO 4'b1001: SPI1 TX FIFO 4'b1010: I2STXFIFO(I2STX/SPDIFTX) 4'b1011: DAC FIFO0(DAC/I2STX/SPDIFTX) 4'b1100: DAC FIFO1(DAC/I2STX/SPDIFTX) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0
7:5	-	Reserved	R	0x0
4	SAM	Source address mode 0: increment 1: constant	R/W	0x0
3:0	SRCSL	Source Select 4'b0000: memory 4'b0010: SPI2 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: UART1 RX FIFO 4'b0101: SDIO FIFO 4'b0110: SD/MMC FIFO 4'b0111: USB FIFO 4'b1000: SPI0 RX FIFO 4'b1001: SPI1 RX FIFO 4'b1010: I2SRX1FIFO(I2SRX1/SPDIFRX) 4'b1011: ADC FIFO(ADC/I2SRX0) 4'b1111: LCD FIFO Others: Reserved	R/W	0x0

6.4.61 DMA7START

DMA7 Start Register 0, offset = 0x00000804

Bits	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	DMASTART	DMA start bit A low-to-high conversion of this bit will lead to load source address, destination address, DRQ type to the DMA controller. This bit will be automatically cleared by the DMAx controller if the DMAx transmission is complete or DMAx transmission error occurs. This bit can be written '0' to abort DMAx transmission.	R/W	0x0

6.4.62 DMA7SADDR0

DMA7 Source Address Register 0, offset = 0x00000808

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 0 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.63 DMA7SADDR1

DMA7 Source Address Register 1, offset = 0x0000080C

Bits	Name	Description	Access	Reset
31:0	DMASADDR	The source address 1 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 32-bit.	R/W	0x0

6.4.64 DMA7DADDR0

DMA7 Destination Address Register 0, offset = 0x00000810

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 0 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.65 DMA7DADDR1

DMA7 Destination Address Register 1, offset = 0x00000814

Bits	Name	Description	Access	Reset
31:0	DMADADDR	The destination address 1 of DMA7 transmission The bit[0] is no effect if data width is 16-bit. The bit[1..0] is no effect if data width is 32-bit.	R/W	0x0

6.4.66 DMA7BC

DMA7 Byte Counter Register, offset = 0x00000818

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMABYTECOUNTER	The byte counter of DMA7 transmission	R/W	0x0

6.4.67 DMA7RC

DMA7 Remain Byte Counter Register, offset = 0x0000081C

Bits	Name	Description	Access	Reset
31:18	-	Reserved	R	0x0
17:0	DMAREMAINCOUNTER	The remain counter length of DMA7 transmission	R/W	0x0

7 PMU

7.1 Features

The ATS2835P integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery and DC5V power supply
- Integrated DC-DC buck converters output 1.5V
- Linear regulators outputs AVCC from VCC, and VDD from VD15

7.2 Module Description

7.2.1 DC-DC Converter

The DC-DC converter efficiently scales battery voltage to the required supply voltage. It can work in Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM) automatically for different load current. The DC-DC converters include several advanced features:

- Input power from SYSPOWER
- Synchronization DC-DC converter architecture
- Programmable output voltages 1.0~1.65V
- Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current.
- Support 2.2uH ~ 4.7uH power inductor, support soft start.

7.2.2 Linear Regulators

7.2.2.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within ±5%, providing maximum output currents when voltages drop to 95%. Table7-1 shows data of maximum output current.

Table 7-1 Regulators Maximum Output Current

Block Name	Output Voltage	Load Capacity
VCC	2.7~3.4V	300 mA
VDD	0.8~1.5V	70 mA@98%
AVCC	VCC-0.15V	50 mA@98%

7.2.2.2 Regulators Power Down

If the system is to operate from an external power supply, then the internal linear regulators are powered down automatically.

7.2.3 Reference Voltage

There is a build-in 1.5V-reference voltage output—VREFI.

7.2.4 A/D Converters

There are 10 bits A/Ds for system monitor, the input voltage range of which is 0V to SVCC @ LRADC2~11 pin , 1.1V to 4.8V at VBAT pin, 0V to 6.0V at DC5V pin, 0V to SVCC at LRADC1 pin ,-40~120℃ for temp sensor.
For LRADC1~11, 1LSB = 3.6V/(2^10) = 3.52mV;
For BATADC, 1LSB = 4.8V/(2^10) =4.69mV;
For DC5V, 1LSB = 6V/(2^10) = 5.86mV;

For SENSADC, T=160/1024*data (decimal) - 40℃;
When the input voltage is V, the related ADC data n = V/(3.6/2^10).

7.3 PMU Register List

Table 7-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address
PMU	0xC0020000	0xC0020000

Table 7-3 PMU Block Configuration Registers List

Offset	Register Name	Description
0x14	WKEN_CTL	Wake up source enable Register
0x18	WAKE_PD	Wake up pending control Register
0x1C	ONOFF_KEY	On/off KEY control Register
0x44	VOUT_CTL	VCC/VDD/AVCC voltage set Register
0x48	MULTI_USED	multi-used set Register
0x50	PMUADC_CTL	PMU ADC frequency and enable Register
0x54	BATADC_DATA	BATADC data Register
0x58	TEMPADC_DATA	TEMPADC data Register
0x5C	DC5VADC_DATA	DC5V ADC data Register
0x60	SENSADC_DATA	Sensor ADC DATA Register
0x64	LRADC1_DATA	LRADC1 data Register
0x68	LRADC2_DATA	LRADC2 data Register
0x6C	LRADC3_DATA	LRADC3 data Register
0x70	LRADC4_DATA	LRADC4 data Register
0x74	LRADC5_DATA	LRADC5 data Register
0x78	LRADC6_DATA	LRADC6 data Register
0x7C	LRADC7_DATA	LRADC7 data Register
0x80	LRADC8_DATA	LRADC8 data Register
0x84	LRADC9_DATA	LRADC9 data Register
0x88	LRADC10_DATA	LRADC10 data Register
0x8C	LRADC11_DATA	LRADC11 data Register
0x90	AVCCADC_DATA	AVCCADC data Register

7.4 PMU Register Description

7.4.1 WKEN_CTL

Wake up source enable Register, offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved	R	0x0
13	IRC_WK_EN	IRC wake-up enable bit 0: Disable 1: Enable	R/W	0x1
12	BAT_WK_EN	battery insertion wake-up enable bit 0: Turn off battery insertion wake-up 1: Open battery insertion detection	R/W	0x1
11	REMOTE_WK_EN	Wire-control wake-up enable bit	R/W	0x1

		0: Turn off wire-control wake-up 1: Open wire-control wake-up		
10	UVLOWPD_SEL	DC5V wake-up condition 0: DC5V>BAT+0.1V 1: DC5V>BAT+0.02V	R/W	0x1
9	NFC_WK_EN	NFC wake-up enable bit 0: Disable 1: Enable	R/W	0x1
8	HDSW_BLOCK	Toggle switch shields long/short press on play key to wakeup enable release bit 0: Toggle switch turn to OFF will shield long/shot press on the play key to wake up 1: Toggle switch do not shield long/short press on the play key to wake up	R/W	0x0
7	HDSWOFF_EN	Toggle switch power off enable bit in sniff status 0: Disable 1: Enable	R/W	0x1
6	BT_WK_EN	Bluetooth wake-up enable bit 0: Disable 1: Enable	R/W	0x1
5	DC5VOFF_WK_EN	DC5V was pulled up wake-up enable bit 0: Disable 1: Enable	R/W	0x0
4	DC5VON_WK_EN	DC5V was pulled in wake-up enable bit 0: Disable 1: Enable	R/W	0x1
3	RESET_WK_EN	RESET wake-up enable bit 0: Disable 1: Enable	R/W	0x1
2	SHORT_WK_EN	ONOFF was short press wake-up enable bit 0: Disable 1: Enable	R/W	0x0
1	LONG_WK_EN	ONOFF was long press wake-up enable bit 0: Disable 1: Enable	R/W	0x1
0	HDSW_WK_EN	HDSW toggle switch wake-up enable bit 0: Disable 1: Enable	R/W	0x1

7.4.2 WAKE_PD

WAKE up pending control Register, offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R/W	0x0
23	LB_PD	Battery low power protection pending bit 0: Battery low power did not happen 1: The battery is low power Write “1” to clear this bit.	R/W	0x0
22:20	-	Reserved	R/W	0x0
19	DC5VRST_PD	DC5V reset pending 0: no DC5V reset 1: DC5V reset happened Write “1” to clear this bit.	R/W	0x0

18:16	-	Reserved	R/W	0x0
15	ONOFF_L_PD	Long press on ONOFF key pending bit 0: no long press on ONOFF key 1: long press on ONOFF key happened Write “1” to clear this bit.	R/W	0x0
14	ONOFF_S_PD	Short press on ONOFF key pending bit 0: no short press on ONOFF key 1: short press on ONOFF key happened Write “1” to clear this bit.	R/W	0x0
13	IRC_WK_PD	IRC wakeup pending bit 0: no IRC wakeup 1: IRC wakeup happened Write “1” to clear this bit.	R/W	0x0
12	BAT_PD	Battery insert wakeup pending bit 0: no battery insert wakeup 1: battery insert wakeup happened Write “1” to clear this bit.	R/W	0x0
11	REMOTE_PD	Drive-by-wire control wakeup pending bit 0: no Drive-by-wire control wakeup 1: Drive-by-wire control wakeup happened Write “1” to clear this bit.	R/W	0x0
10	-	Reserved	R/W	0x0
9	NFC_PD	NFC Pending 0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	R/W	0x0
8	-	Reserved	R/W	0x0
7	HDSWOFF_PD	Toggle switch OFF pending bit 0: no toggle switch operation 1: toggle switch OFF operation happened Write “1” to clear this bit.	R/W	0x0
6	BT_WK_PD	Bluetooth Pending 0: Interrupt source is not active. 1: Interrupt source is active. Writing ‘1’ to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	R/W	0x0
5	DC5VOFF_PD	DC5V pull out pending bit 0: no DC5V pull out 1: DC5V pull out happened Write “1” to clear this bit.	R/W	0x0
4	DC5VON_PD	DC5V pull in pending bit 0: no DC5V pull in 1: DC5V pull in happened Write “1” to clear this bit.	R/W	0x0
3	-	Reserved	R/W	0x0
2	SHORT_WK_PD	Short press ONOFF wakeup pending bit 0: no short press 1: short press happened Write “1” to clear this bit.	R/W	0x0
1	LONG_WK_PD	Long press ONOFF wakeup pending bit 0: no long press	R/W	0x0

		1: long press happened Write “1” to clear this bit.		
0	HDSWON_PD	Toggle switch ON pending bit 0: no toggle switch operation 1: toggle switch ON operation happened Write “1” to clear this bit.	R/W	0x0

7.4.3 ONOFF_KEY

ONOFF key control & detect register, offset = 0x1C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R/W	x
10	RESTART_SET	Set up RESET key function 0: reset VDD power domain registers 1: restart, system enters standby after pressing reset (Debounce 16ms), and waked up to active after lifting up the key.	R/W	0x0
9:7	ONOFF_PRESS_TIME	Set up ONOFF keystroke duration 000: 50ms < t < 0.125s, short press; t >=0.125s, long press. 001: 50ms < t < 0.25s, short press; t >=0.25s, long press. 010: 50ms < t < 0.5s, short press; t >=0.5s, long press. 011: 50ms < t < 1s, short press; t >=1s, long press. 100: 50ms < t < 1.5s, short press; t >=1.5s, long press. 101: 50ms < t < 2s, short press; t >=2s, long press. 110: 50ms < t < 3s, short press; t >=3s, long press. 111: 50ms < t < 4s, short press; t >=4s, long press.	R/W	0x1
6	ONOFF_RST_EN	Enable long press ONOFF to reset 0: Disable 1: Enable	R/W	0x1
5:4	ONOFF_RST_T_SEL	Long press ONOFF to send reset signal time 00: 8s 01: 12s 10: 16s 11: 24s	R/W	0x0
3	ONOFF_STATE	Toggle switch status machine indicator bit 0: 2⁄3 status (OFF status) 1: 1⁄3 status (ON status)	R	0x1
2	HDSWOFF_2_3	ONOFF electrical level 0: Not at this electrical level 1: at 2⁄3 electrical level	R	0x0
1	HDSWON_1_3	ONOFF electrical level 0: Not at this electrical level 1: at 1⁄3 electrical level	R	0x0
0	ONOFF_PRESS_0	ONOFF key pressed indicator bit 0: ONOFF key was not pressed	R	0x0

		1: ONOFF key was pressed		

7.4.4 VOUT_CTL

Voltage set register, offset=0x44

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	R/W	0x0
20	SPLL_AVDD_EN	SPLL_AVDD LDO Enable 0: Disable 1: Enable	R/W	0x0
19	SPLL_AVDD_VOL_SET	SPLL_AVDD Voltage Set 0: 1.1V 1: 1.2V	R/W	0x1
18	AVDD_PD	AVDD capacitor-less LDO pull-down 0: no pull-down 1: 1mA pull-down	R/W	0x1
17:16	AVDD_VOL	00: 1.0V 01: 1.1V 10: 1.2V 11: 1.3V	R/W	0x2
15	AVCC_BIASEN	AVCC_BIAS SET 0: small current 1: big current	R/W	0x0
14:13	AVCC_DROP	AVCC LDO margin tuning, voltage drop from VCC ***00: 0.15V 01: 0.20V 10: 0.25V 11: 0.30V	R/W	0x0
12	VCCOC_SET	VCC LDO Current limit 0: 400mA 1: 500mA	R/W	0x0
11	VDDOC_SET	VDD LDO Current limit 0: 200mA 1: 300mA	R/W	0x0
10:8	VCC_SET	VCC voltage level select 000: 2.7V 001: 2.8V 010: 2.9V 011: 3.0V *100: 3.1V 101: 3.2V 110: 3.3V 111: 3.4V	R/W	0x4
7:4	VDD_SET_S1	VDD(Regulator) voltage coarse control (S1) 0000: 0.80V 0001: 0.85V 0010: 0.9V 0011: 0.95V 0100: 1.0V 0101: 1.05V 0110: 1.1V 0111: 1.15V *1000: 1.2V	R/W	0x8

		1001: 1.25V 1010: 1.3V 1011: 1.35V 1100: 1.4V 1101: 1.45V 1111: 1.5V		
3:0	VDD_SET_S3BT	VDD(Regulator) voltage coarse control (S3BT) 0000 0.80V 0001 0.85V *0010 0.9V 0011 0.95V 0100 1.0V 0101 1.05V 0110 1.1V 0111 1.15V 1000 1.2V 1001 1.25V 1010 1.3V 1011 1.35V 1100 1.4V 1101 1.45V 1111 1.5V	R/W	0x2

7.4.5 MULTI_USED

Multi Use register, offset=0x48

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14	UVLO_T	Debounce time selection for UVLO indication 0: 41us 1: 16ms	R/W	0x1
13:10	-	Reserved	R	0x0
9	UVLO	DC5V pull-in detection condition 0: no DC5V pull-in detection 1: DC5V>BAT+0.1V or DC5V>BAT+0.02V	R	x
8	UVDD_EN	USBVDD LDO enable 0: Disable 1: Enable	R/W	0x0
7:5	UVDD_V	USBVDD LDO output voltage control 000: 1.0V 001: 1.05V 010: 1.1V 011: 1.15V 100: 1.2V 101: 1.25V 110: 1.3V 111: reserved	R/W	0x4
4	USBVDD_PD	USBVDD pull-down resistor enable 0: Disable, no pull-down resistor. 1: Enable, pull-down resistor corresponds to 1mA load current.	R/W	0x0
3	USBVDD_PD2	USBVDD pull-down resistor_2 enable 0: Disable, no pull-down resistor_2. 1: Enable, pull-down resistor_2 corresponds to 5mA	R/W	0x0

		load current.		
2	USBVDD_PD3	USBVDD pull-down resistor_3 enable 0: Disable, no pull-down resistor_3. 1: Enable, pull-down resistor_3 corresponds to 10mA load current.	R/W	0x0
1	SEG_DISP_VCC_EN	Segment screen power enable 0: Disable 1: Enable	R/W	0x0
0	SEG_LED_EN	LED constant current source enable 0: Disable 1: Enable	R/W	0x0

7.4.6 PMUADC_CTL

PMUADC Control Register, offset = 0x50

Bit (s)	Name	Description	Access	Reset
31:18	-	Reserved	R/W	0x0
17	I_COMP_SET	ADC COMP current set 0: 0.5uA 1: 1uA	R/W	0x0
16	COMP_TRIM	COMP trim enable 0: Disable 1: Enable	R/W	0x1
15	LRADC11_EN	LRADC11 A/D enable 0: Disable 1: Enable	R/W	0x0
14	LRADC10_EN	LRADC10 A/D enable 0: Disable 1: Enable	R/W	0x0
13	LRADC9_EN	LRADC9 A/D enable 0: Disable 1: Enable	R/W	0x0
12	LRADC8_EN	LRADC8 A/D enable 0: Disable 1: Enable	R/W	0x0
11	LRADC7_EN	LRADC7 A/D enable 0: Disable 1: Enable	R/W	0x0
10	LRADC6_EN	LRADC6 A/D enable 0: Disable 1: Enable	R/W	0x0
9	LRADC5_EN	LRADC5 A/D enable 0: Disable 1: Enable	R/W	0x0
8	LRADC4_EN	LRADC4 A/D enable 0: Disable 1: Enable	R/W	0x0
7	LRADC3_EN	LRADC3 A/D enable 0: Disable 1: Enable	R/W	0x0
6	LRADC2_EN	LRADC2 A/D enable 0: Disable 1: Enable	R/W	0x0

5	LRADC1_EN	LRADC1 A/D enable 0: Disable 1: Enable	R/W	0x1
4	SENSORADC_EN	sensor A/D enable 0: Disable, sensor circuit and output disable 1: Enable, sensor circuit and output enable	R/W	0x0
3	DC5VADC_EN	DC5V A/D enable 0: Disable 1: Enable	R/W	0x1
2	TEMPADC_EN	TEMP A/D enable 0: Disable 1: Enable	R/W	0x1
1	BATADC_EN	Battery A/D enable 0: Disable 1: Enable	R/W	0x1
0	AVCCADC_EN	AVCC A/D enable 0: Disable 1: Enable	R/W	0x1

7.4.7 BATADC_DATA

BATADC DATA Register, offset = 0x54

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	BATADC	10bit Voltage ADC, used to detect Battery voltage. Input Li-ion voltage range is 1.5-4.5V.	R	xx

7.4.8 TEMPADC_DATA

TEMPADC DATA Register, offset = 0x58

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	TEMPADC	10bit Voltage ADC, used to detect TEMPADC voltage. Input voltage range is 0-3.6V.	R	xx

7.4.9 DC5VADC_DATA

DC5V ADC DATA Register, offset = 0x5C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	DC5VADC	10bit Voltage ADC, used to detect DC5V voltage. Input voltage range is 0-6V.	R	xx

7.4.10 SENSADC_DATA

Sensor ADC DATA Register, offset = 0x60

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	SENSADC	10bit Voltage ADC, used to detect TEMPSENSOR voltage.	R	xx

7.4.11 LRADC1_DATA

LRADC1 DATA Register, offset = 0x64

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC1	LRADC1 data output LRADC1 input voltage range is 0 to SVCC.	R	xx

7.4.12 LRADC2_DATA

LRADC2 DATA Register, offset = 0x68

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC2	LRADC2 data output LRADC2 input voltage range is 0 to AVCC.	R	xx

7.4.13 LRADC3_DATA

LRADC3 DATA Register, offset = 0x6C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC3	LRADC3 data output LRADC3 input voltage range is 0 to AVCC.	R	xx

7.4.14 LRADC4_DATA

LRADC4 DATA Register, offset = 0x70

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC4	LRADC4 data output LRADC4 input voltage range is 0 to AVCC.	R	xx

7.4.15 LRADC5_DATA

LRADC5 DATA Register, offset = 0x74

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC5	LRADC5 data output LRADC5 input voltage range is 0 to 3.6V.	R	xx

7.4.16 LRADC6_DATA

LRADC6 DATA Register, offset = 0x78

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC6	LRADC6 data output LRADC6 input voltage range is 0 to 3.6V.	R	xx